Scalability Revisited: 100 nm PD-SOI Transistors and Implications for 50 nm Devices

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Outline

- Introduction
- 0.18µm transistor results
- 0.18µm ring oscillator results
- 0.18µm SOI summary
- Scaling trends
- Implications for 0.10µm generation
- Conclusions

Introduction

- Partially Depleted SOI CMOS is receiving attention due to its performance advantages over bulk CMOS
  - Minimal area junction capacitance
  - Floating Body (Gate-Body coupling effect)
  - Absence of body effect in stack circuits
- What is the SOI performance gain for the 0.18μm generation?
- How does SOI performance gain scale to the 0.10μm generation?

Experiment

- Compare performance of SOI and bulk CMOS devices in Intel's 0.18μm technology*

- SOI devices fabricated on SIMOX wafers with final silicon layer and buried oxide thickness of 190 nm

- SOI devices optimized for high performance at matched off current

*** Yang et al., IEDM 1998**

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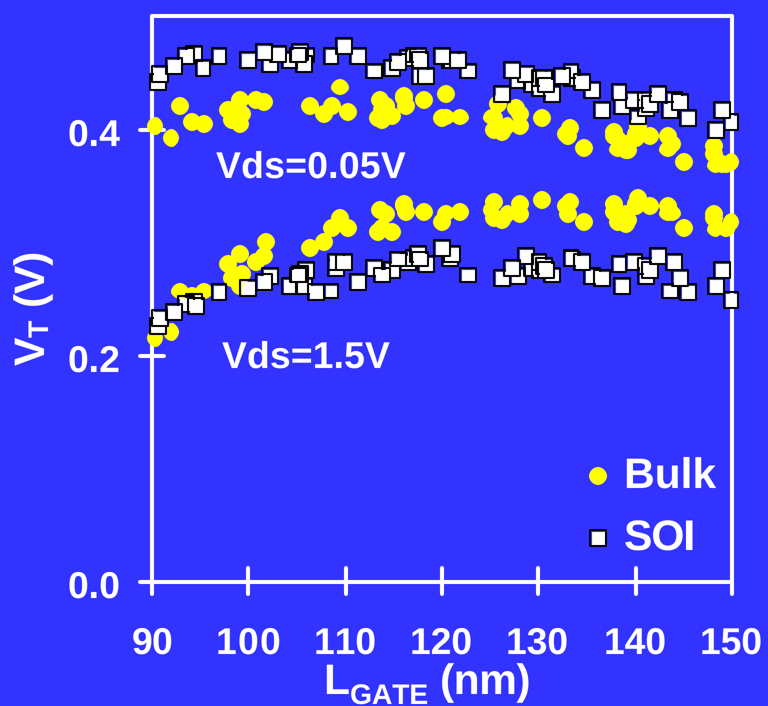
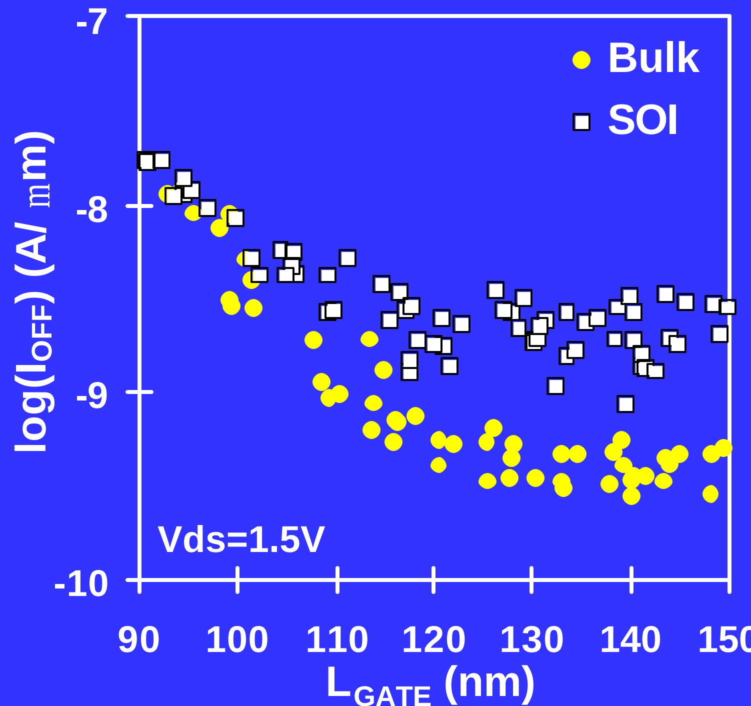
Matched Off Current for NMOS

- I_{OFF} and saturated V_T matched at 100 nm gate length
  - SOI requires 40-50mV higher linear V_T due to floating body





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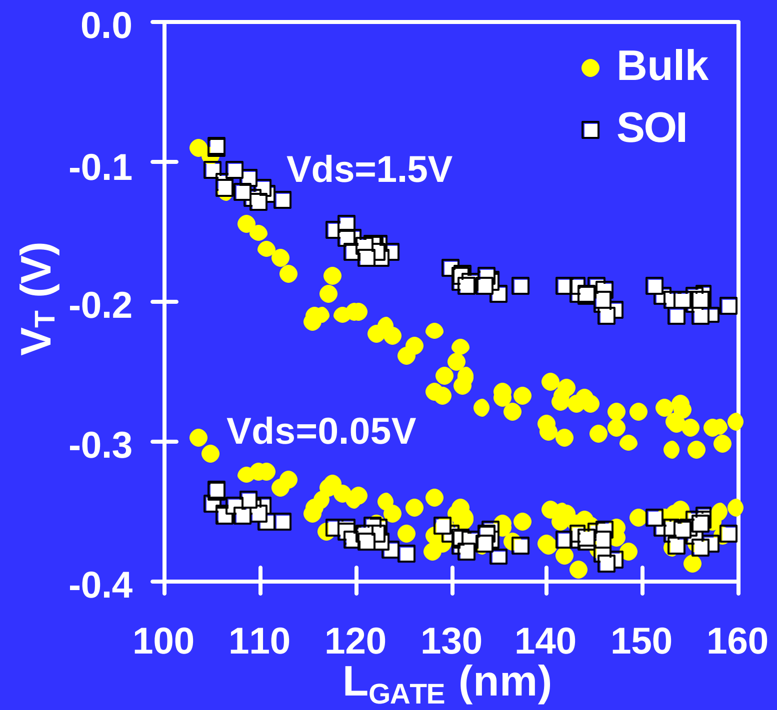
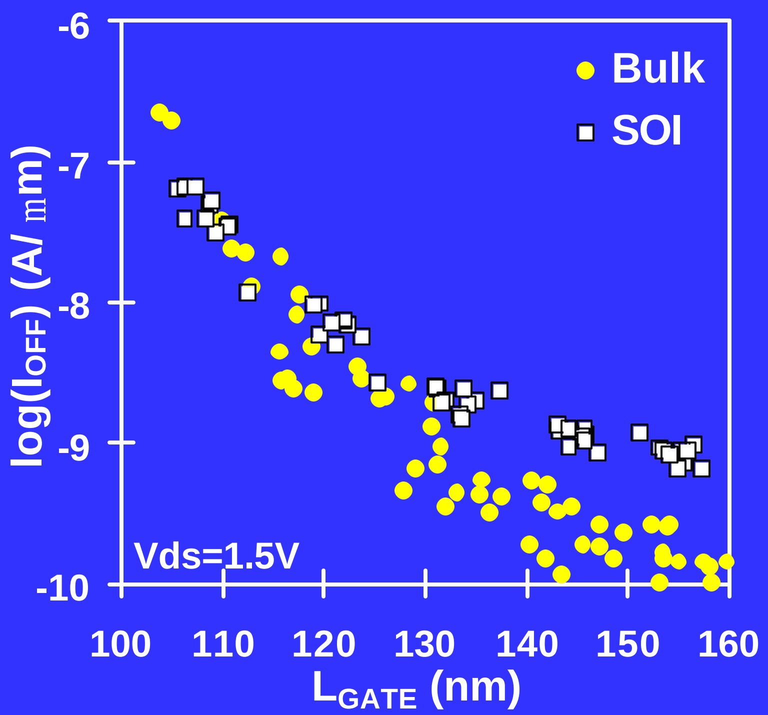
Matched Off Current for PMOS

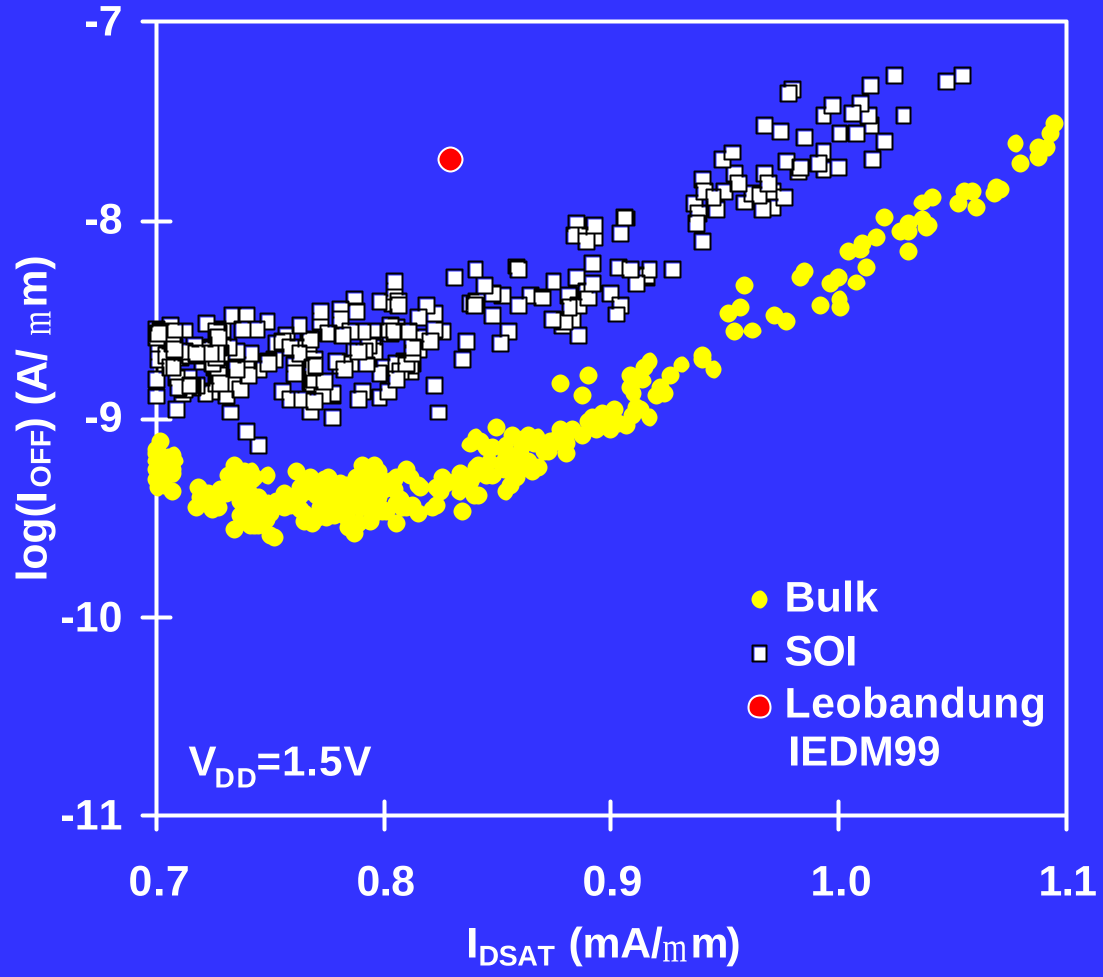
- I_{OFF} and saturated V_T matched at 110 nm gate length
  - SOI requires 20-30mV higher linear V_T due to floating body





NMOS I_{ON} vs. I_{OFF}

- Record 0.18μm generation SOI with 15% higher NMOS I_{DSAT}
- SOI I_{DSAT} 9% lower than bulk, of which 6% is self heat



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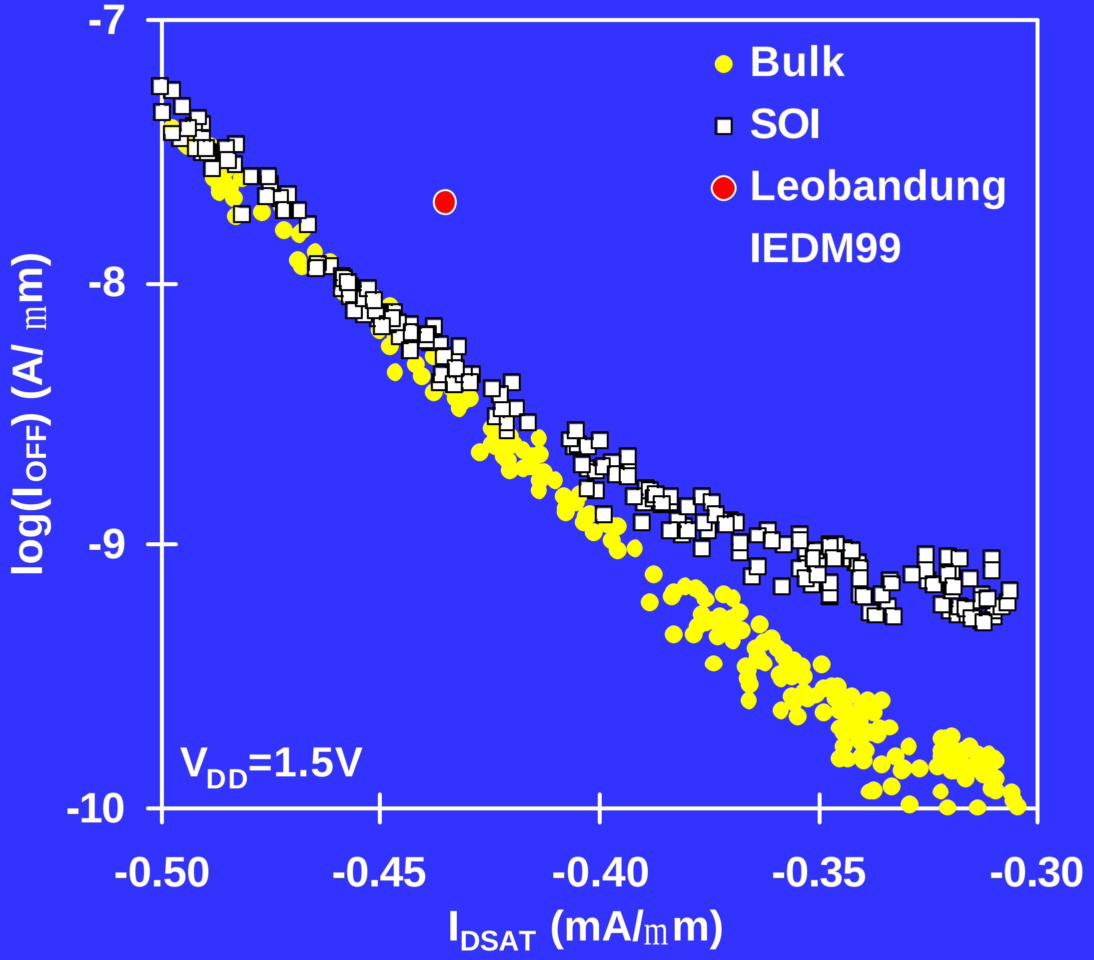
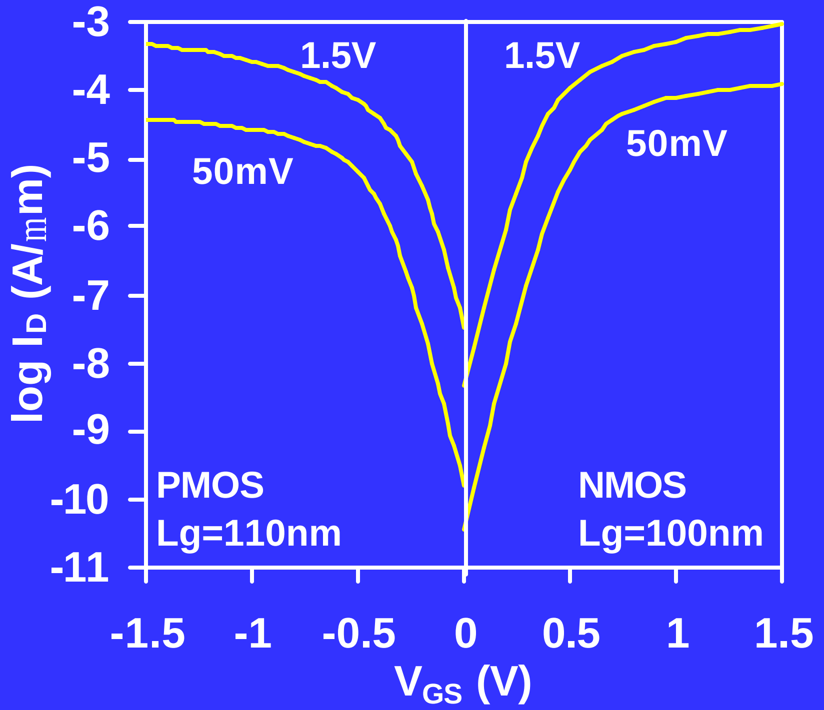
PMOS I_{ON} vs. I_{OFF}

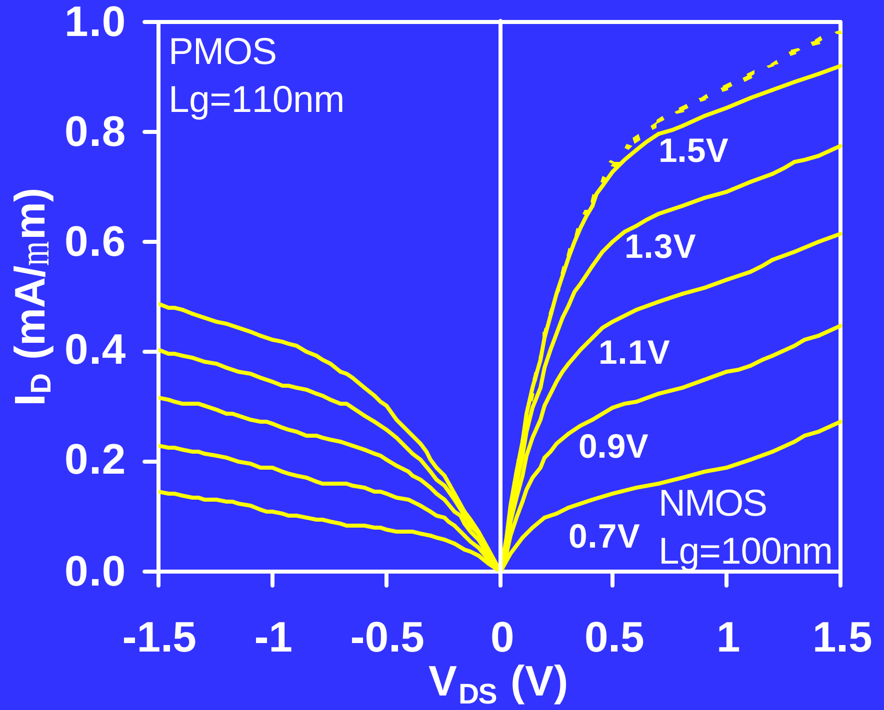
- Record 0.18μm generation SOI with 10% higher PMOS I_{DSAT}



Transistor I-V Characteristics

- Well-behaved SOI device characteristics
  - Self-Heat: NMOS shows ~6% higher I_{DSAT} with pulsed I-V





Transistor Parameter Summary

		Bulk		SOI	
		NMOS	PMOS	NMOS	PMOS
V_{DD}	(V)	1.5	1.5	1.5	1.5
L_{GATE}	(nm)	100	110	100	110
$T_{OX,E}$	(nm)	3	3	3	3
V_T (lin)	(mV)	420	-320	**460**	**-350**
V_T (sat)	(mV)	280	-140	270	-140
I_{DSAT}	(µA/µm)	1000	490	**910/970***	490
I_{OFF}	(nA/µm)	5	30	5	30

*SOI I_{DSAT} pulsed I-V

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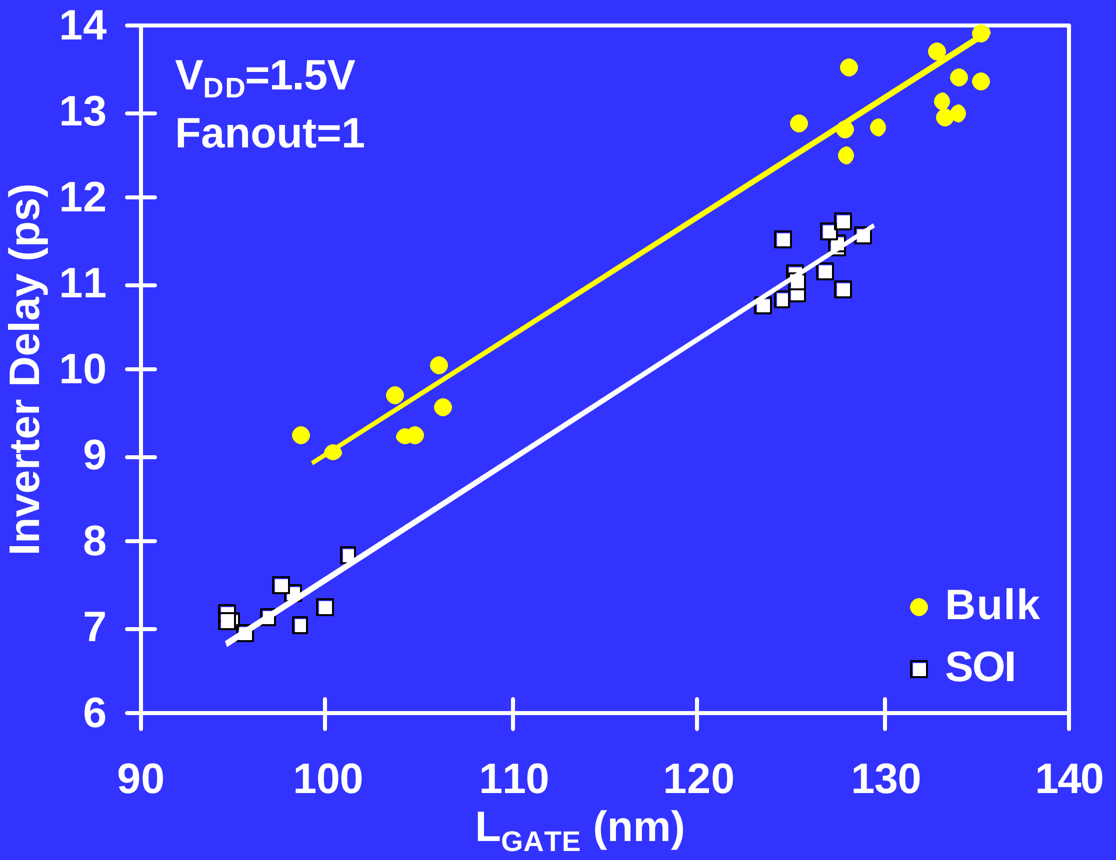
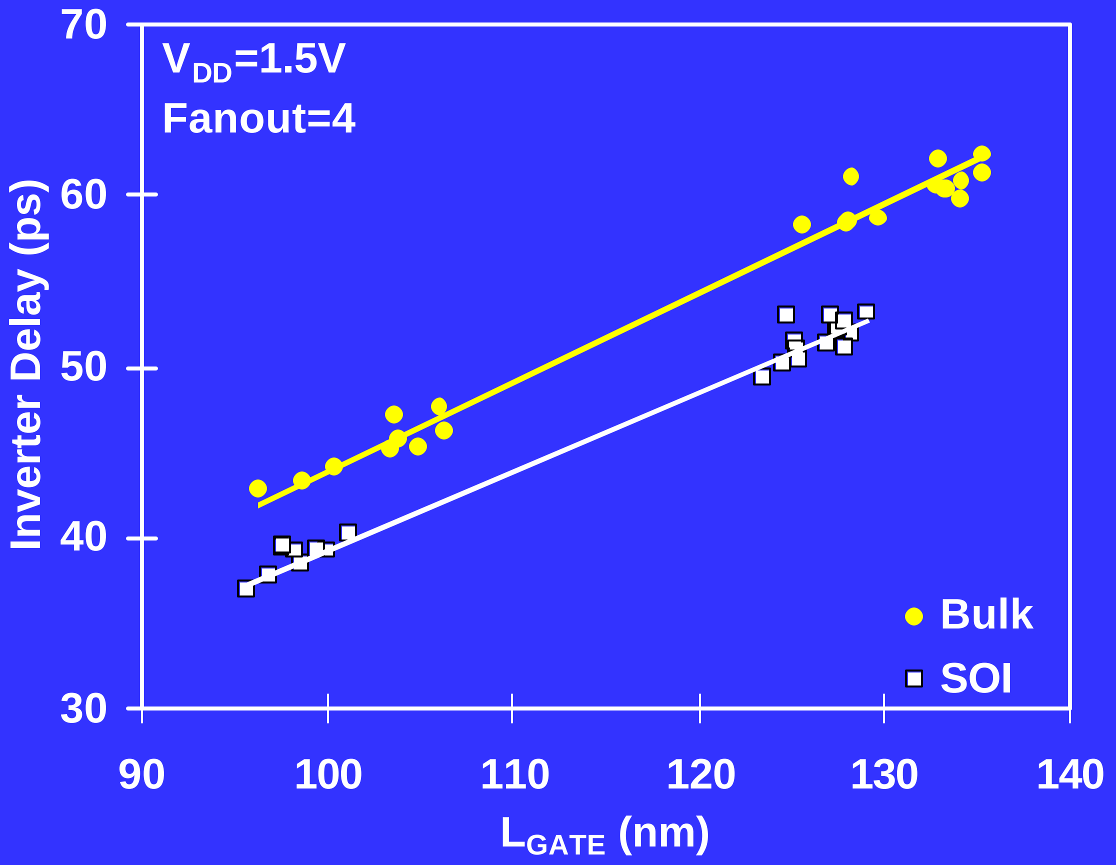
Ring Oscillator: Fanout=1

- 7.4pS SOI delay equals the best reported for 0.18µm
- SOI 16% faster than bulk
  - 5% G-B coupling
  - 11% Jn. Cap.
- Others have reported 25% gain
  - Jn. Cap. is lower for our bulk



Ring Oscillator: Fanout=4

- Larger Fanout more representative of products
- SOI 8% faster than bulk
  - 5% G-B coupling
  - 3% Jn. Cap.



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0.18μm SOI Summary

- Our 0.18μm generation SOI transistors are the best reported
- SOI I_{DSAT} is 10-15% better than best reported at equivalent I_{OFF}
- Inverter delay of 7.4 ps at 100 nm L_{GATE} equals the best reported

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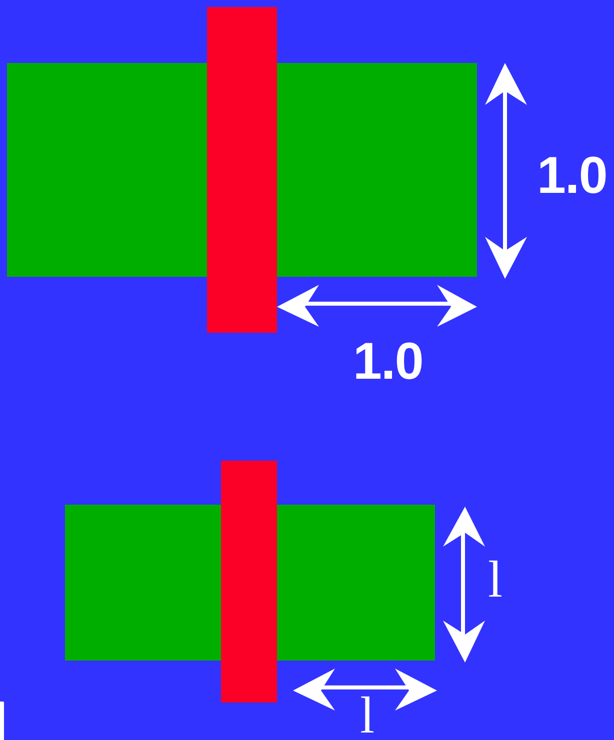
How Does SOI Performance Scale?

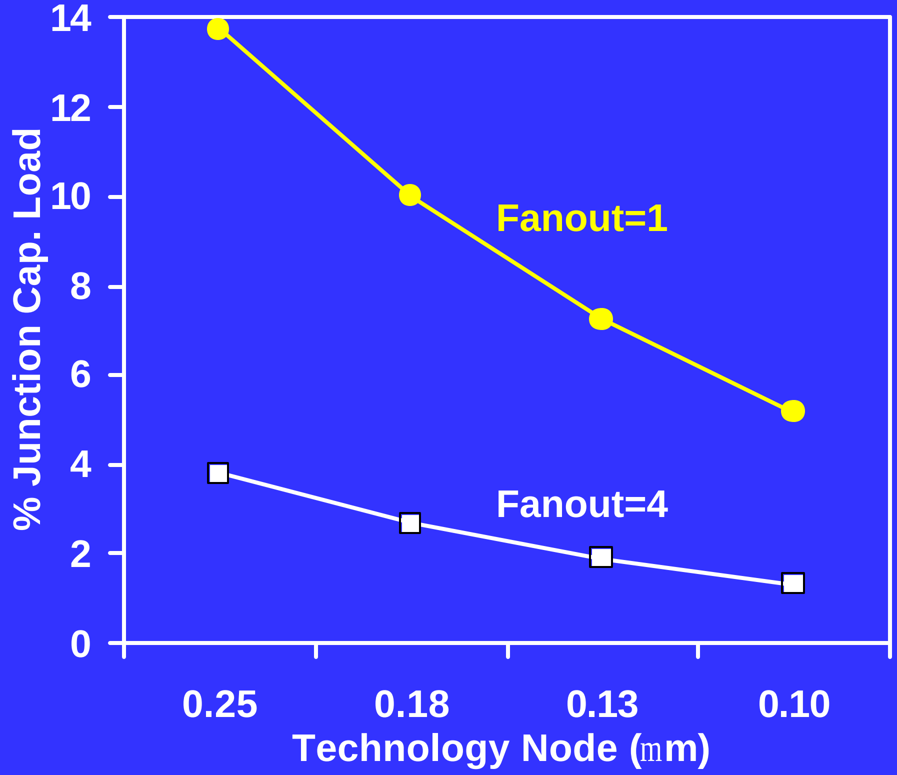
- SOI performance gain over bulk stems from 3 factors
  - Minimal area junction capacitance
  - Floating Body Þ G-B coupling **BUT also History Effect**
  - Absence of body effect in stack circuits

- How do these effects scale to the 0.10µm technology generation?
  - Each of these benefits is diminishing with scaling

Scaling Trend: Junction Capacitance

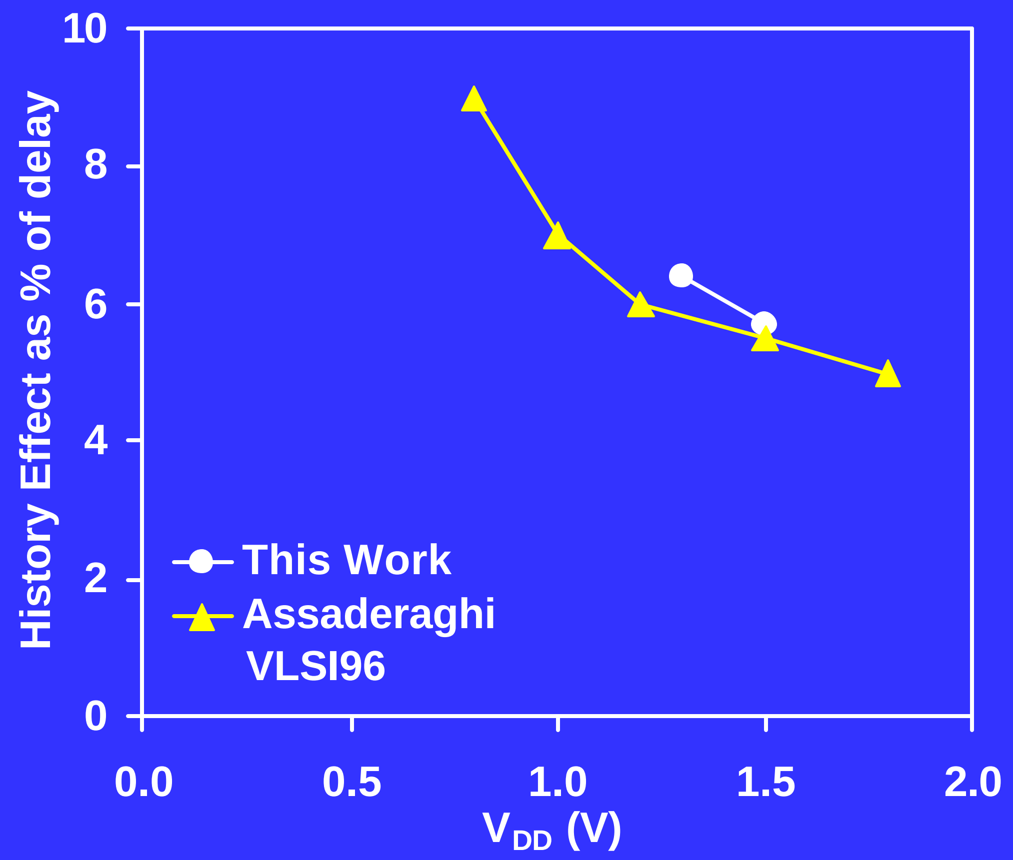
- Role of junction area capacitance reduces with scaling
  - Junction capacitance decreases as λ^2 while gate capacitance decreases as λ





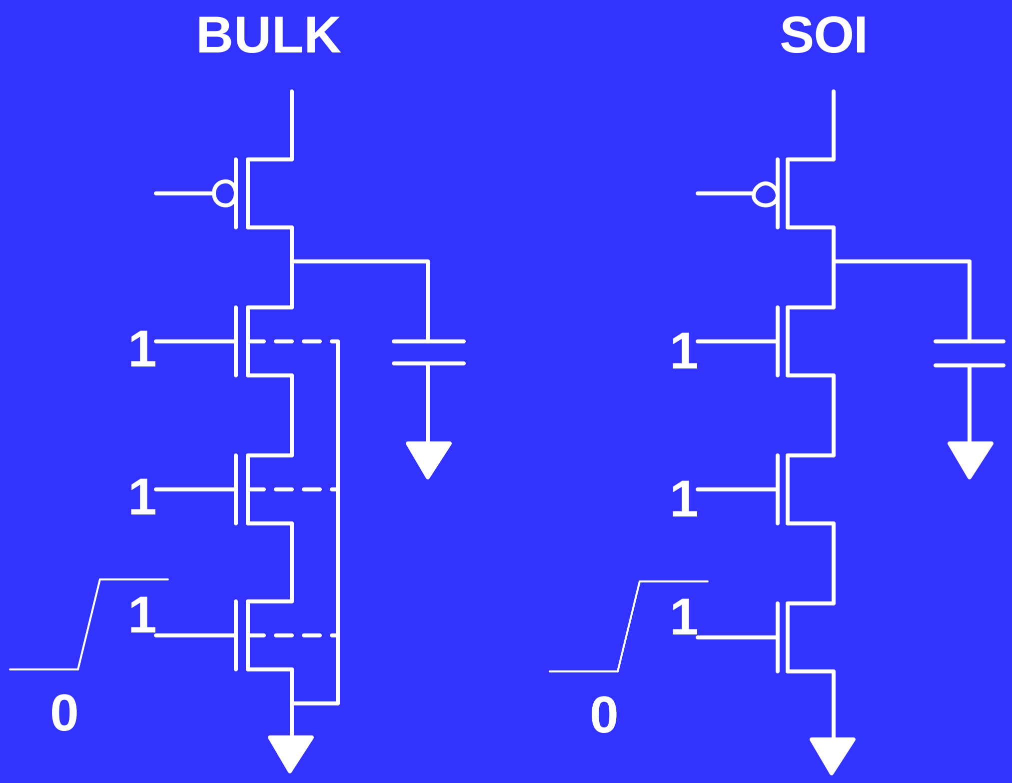
Scaling Trend: History Effect

- Floating body helps SOI performance due to G-B coupling
- However, FB hurts SOI due to history effect
  - V_T of SOI transistor depends on the switching history
  - Bigger effect when $(V_G - V_T)$ is smaller
- Needs to be treated as frequency guardband at product test



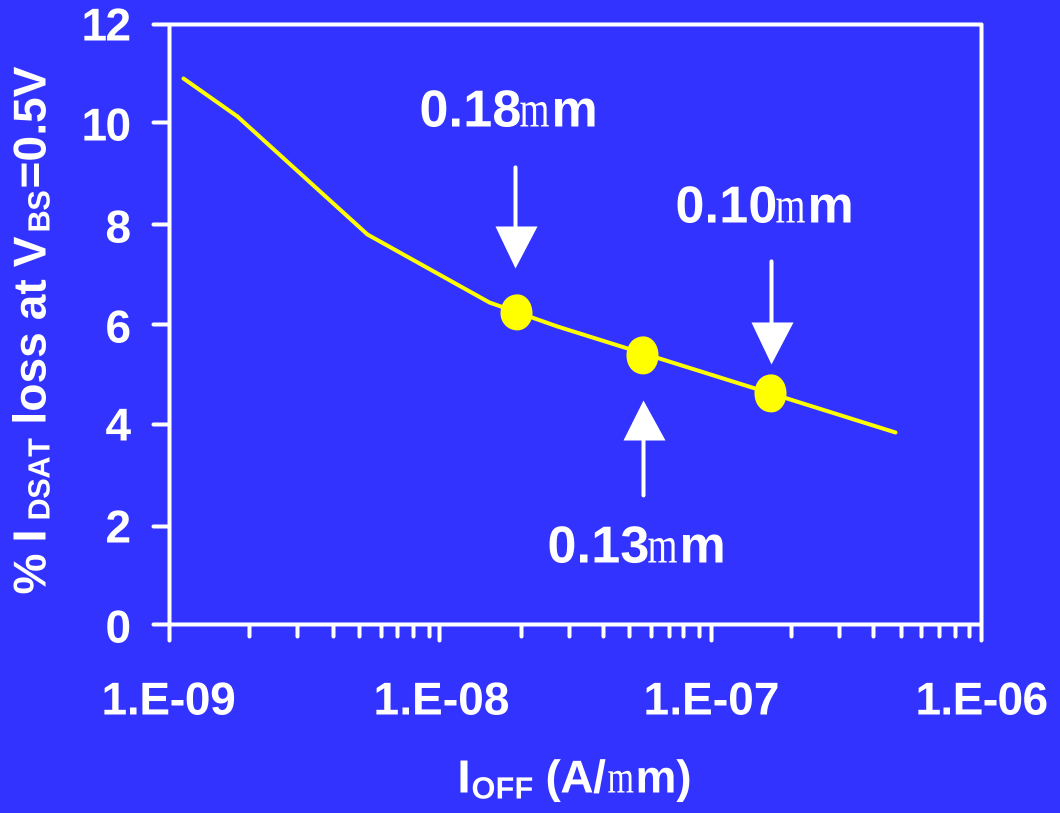
Scaling Trend: Body Effect

- Body Effect reduces performance of stack circuits for bulk CMOS
- SOI does not suffer from this problem since body floats close to source
- Improved SOI delay for stacks:
  - Lower jn. cap.
  - Elimination of the body effect



Scaling Trend: Body Effect

- BUT, body effect in bulk is diminishing as I_{OFF} is increased
- Relative gain for SOI diminished as body effect in bulk CMOS reduces



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Implications for 0.10μm Technology

- All 3 elements of SOI performance diminish with scaling
  - Gain for 0.10μm node: 3-10% depending on history guardband

	0.18um	**0.13um**	**0.10um**
F.O.=1 Inverter	16%	13%	11%
F.O.=4 Inverter	8%	7%	6%
3-Input NAND	20%	17%	14%
Average	**15%**	**12%**	**10%**
History Guardband	-5%	-6%	- 7%
NET	**10%**	**6%**	**3%**

Analysis ignores interconnect load, which reduces SOI gain further

Conclusions

- Record performance 0.18μm generation SOI transistors are reported
  - I_{DSAT} 10-15% better than best reported
  - Inverter delay equal to best reported
- However, SOI performance gain is significantly diminished for the 0.1μm generation due to
  - reduced impact of junction area capacitance
  - increased SOI history effect
  - reduced body effect in stacks for bulk CMOS